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Low-Cost Diode Arrays for Production-Scale Fusion Energy Installations

HECDPSSL
September 12, 2012

Northrop Grumman Cutting Edge Optronics

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Outline

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- Disclaimers…
- NGCEO Overview
- Diode Specifications – LIFE and similar programs
- Potential Diode Package
- What about VCSELs?
- Outlook

Disclaimers…

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- Vantage point – diode lasers
- Most of my information is based on U.S. / LIFE
- Suggested design is just one of many options

NGCEO Overview

- Cutting Edge Optronics is a wholly-owned subsidiary of Northrop Grumman
- Located outside of St. Louis, MO
  - 36,000 ft^2 facility, ~ 90 people
  - All manufacturing and R&D is done at this facility
  - Bar fabrication and packaging since late 1990s

NGCEO Product Overview

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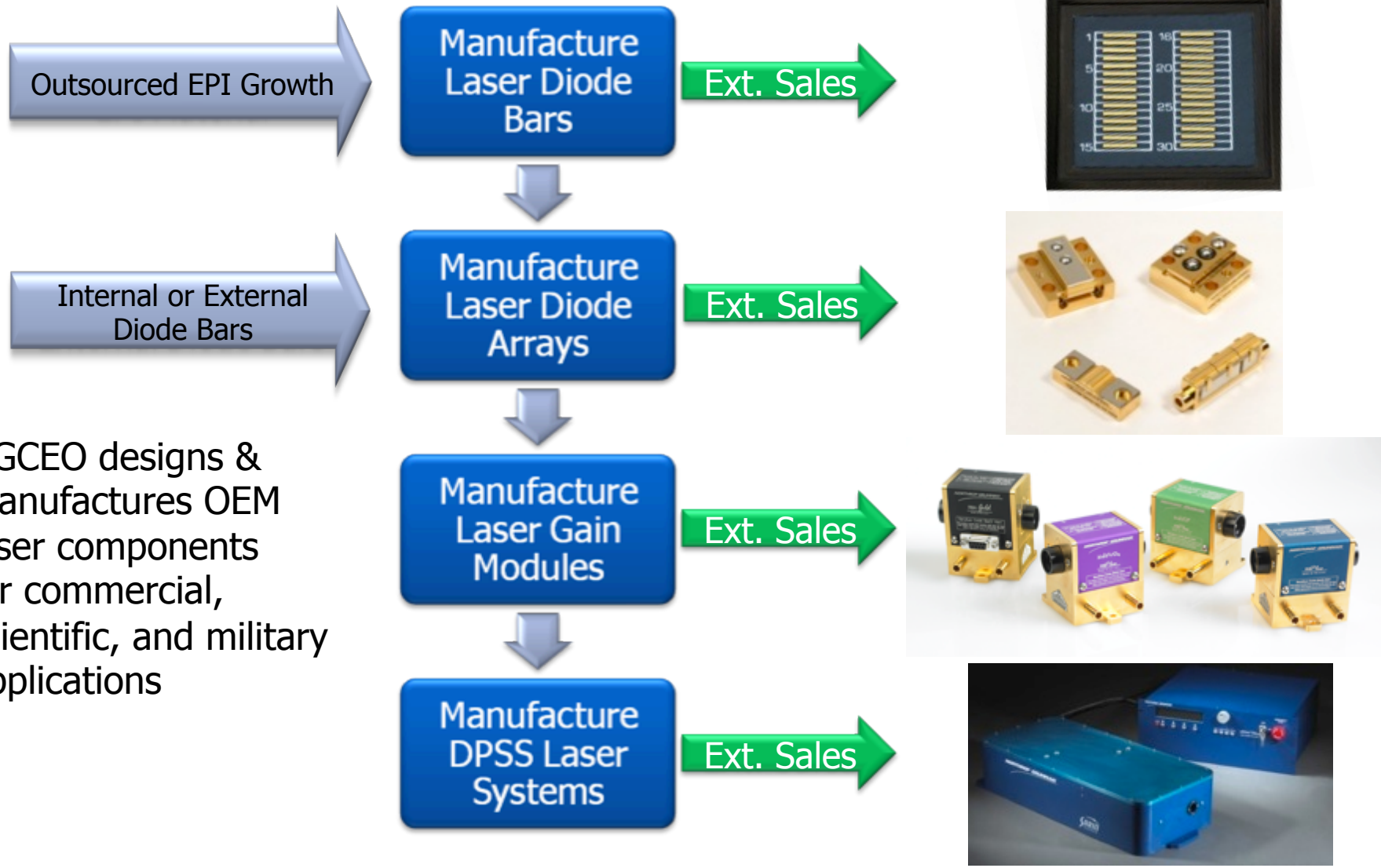

NGCEO designs & manufactures OEM laser components for commercial, scientific, and military applications

DPSS Laser Amplifiers

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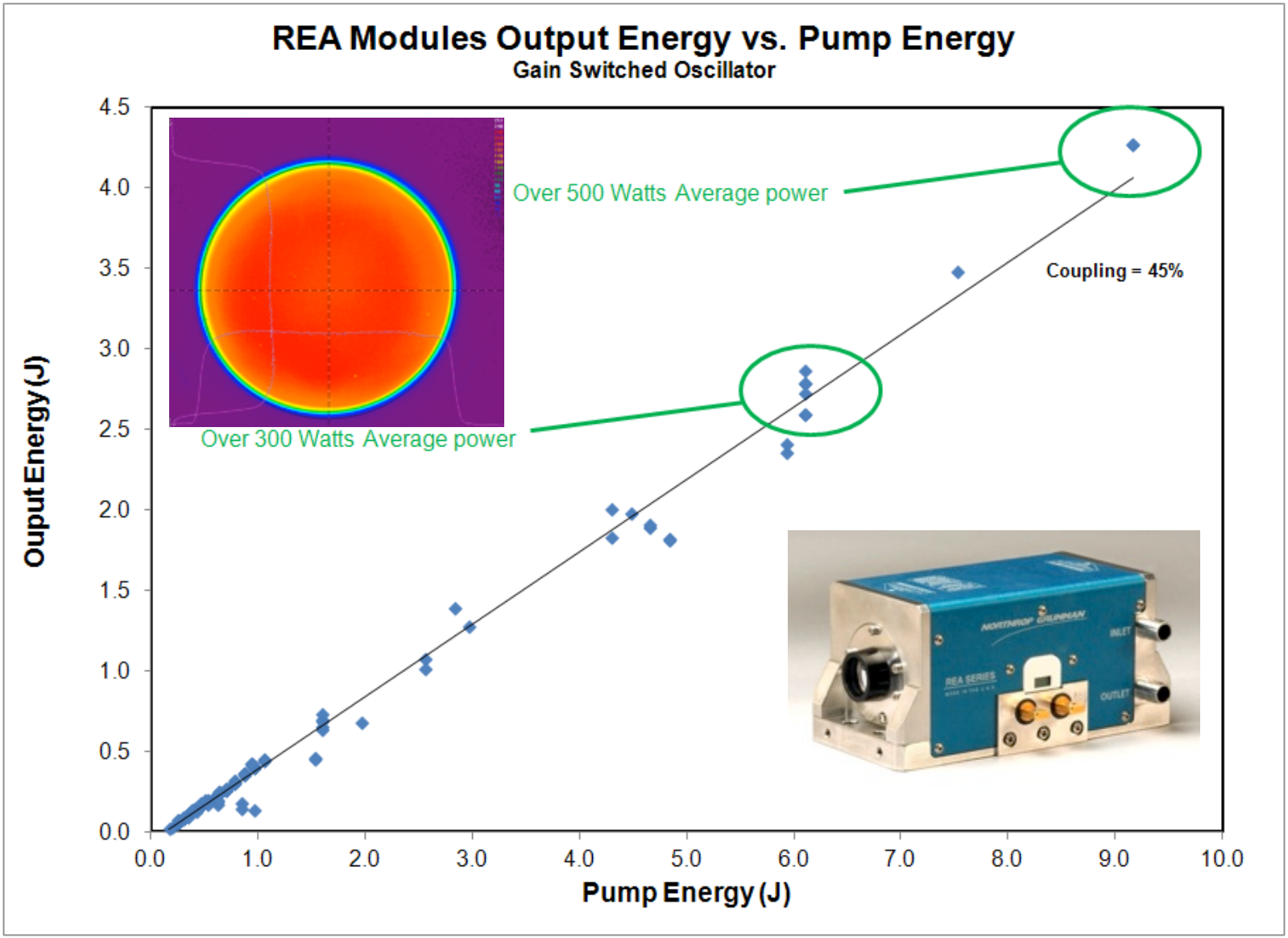

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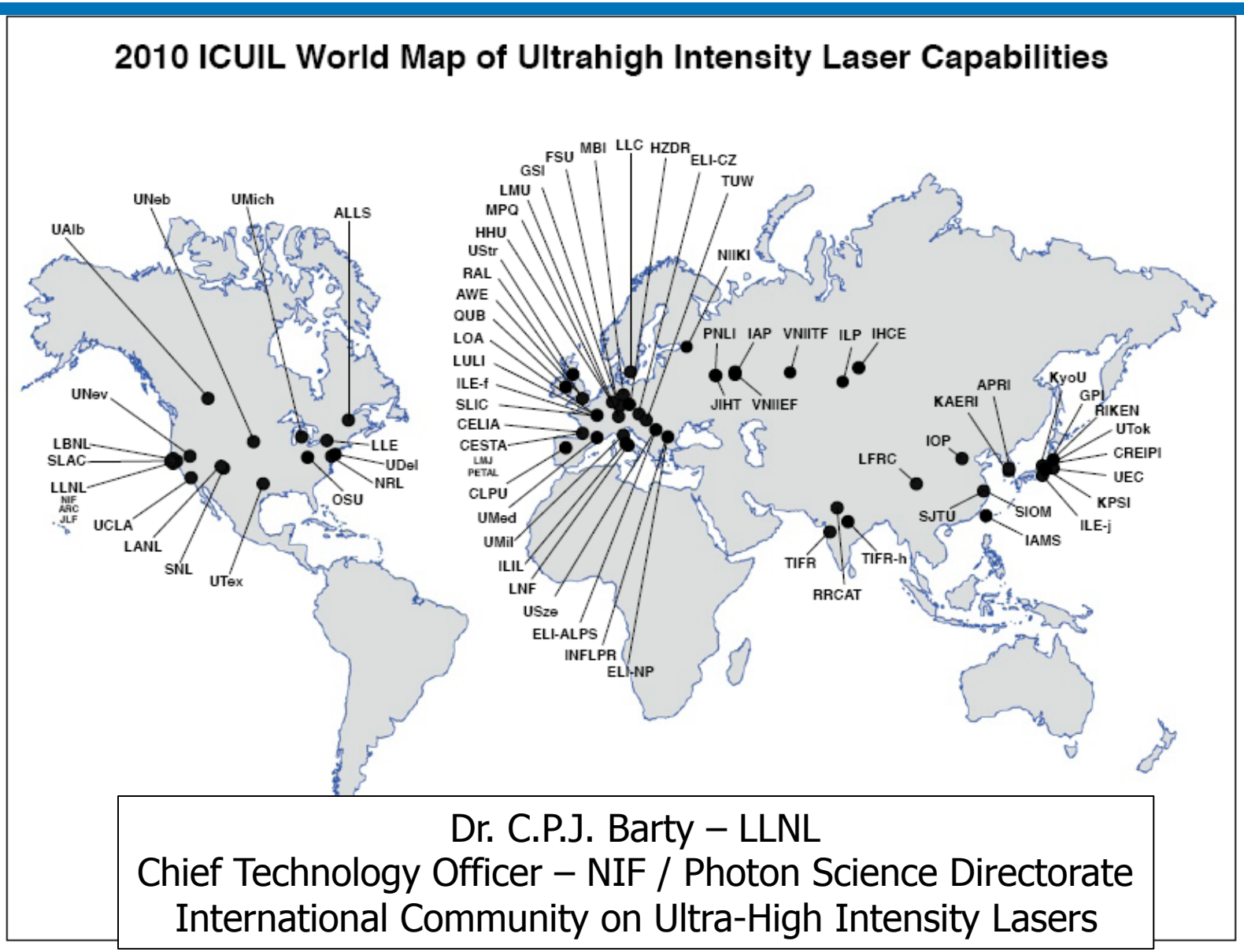
HIGH-INTENSITY LASERS:

DIODE SPECIFICATIONS

High-Intensity Laser Overview



Dr. C.P.J. Barty – LLNL
Chief Technology Officer – NIF / Photon Science Directorate
International Community on Ultra-High Intensity Lasers

NIF ➔ LIFE

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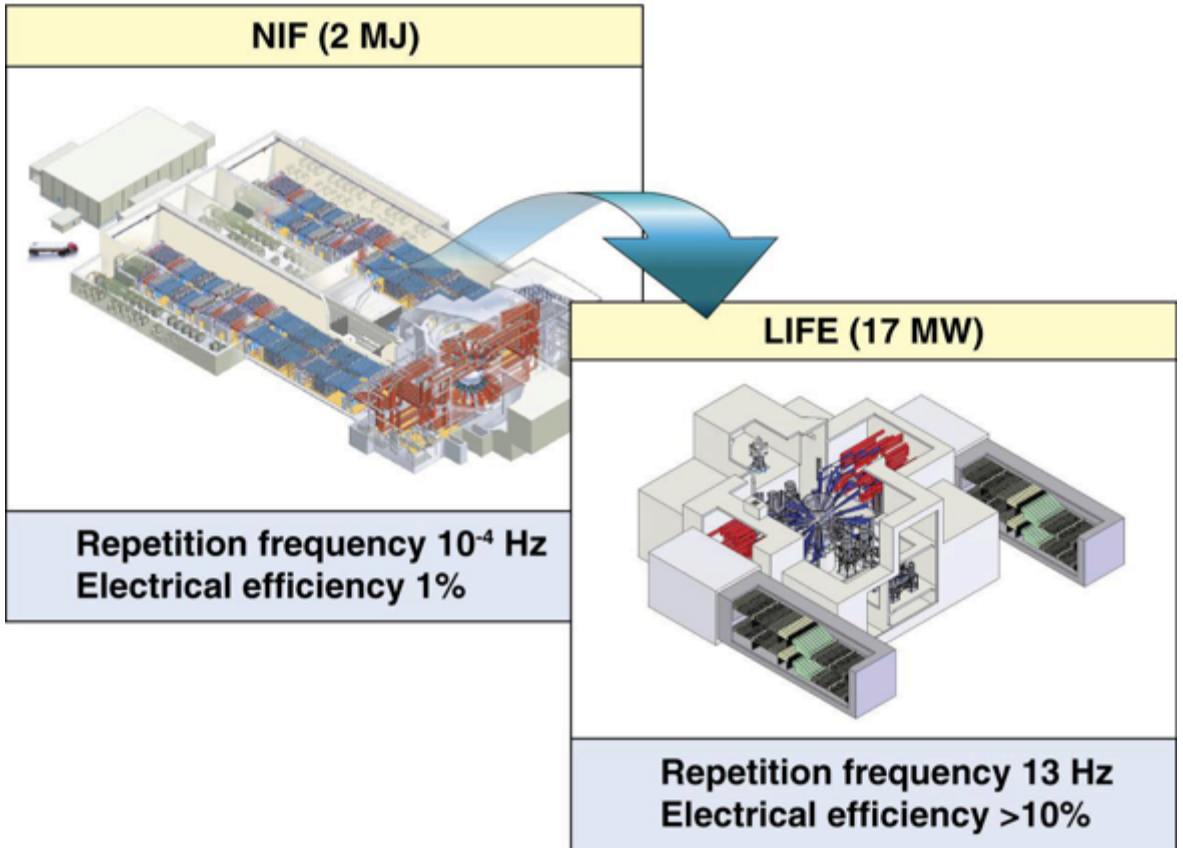
- Lessons learned from NIF provide the framework for LIFE
- Many differences, including the transition from flashlamp pumping to diode pumping
- Diode costs currently represent 30-50% of the entire system cost



LIFE Diode Specifications (Technical)

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Item	Units	Minimum Value	Target Value	Current State / Comments
Intensity	kW/cm^2	10	25	~ 10 (300W @ 350 µm) ~ 22 (300W @ 150 µm) May require 600-700W bar
Efficiency		70%	75%	60-70% (commercial) 70+ (SHEDS, BRIOLAS)
Fast axis divergence	degrees FW 1/e^2	±4	±3	
Slow axis divergence	degrees FWHM	±10	±7	Matches divergence of typical unlensed bar
Wavelength	nm		872	Typical structure
Wavelength spread	nm	±8	±5	
MTTF	Gshots		14	Easily Achievable
Repetition Rate	Hz		15	Low heat ➔ Novel (low-cost) packaging
Pulse Width	µs		200	"
Duty Cycle	%		< 0.5	"
Temperature of mounting plate	°C		5	
Packaging Density				Minimal dead space between diode bars – largest challenge

Now The Hard Part…

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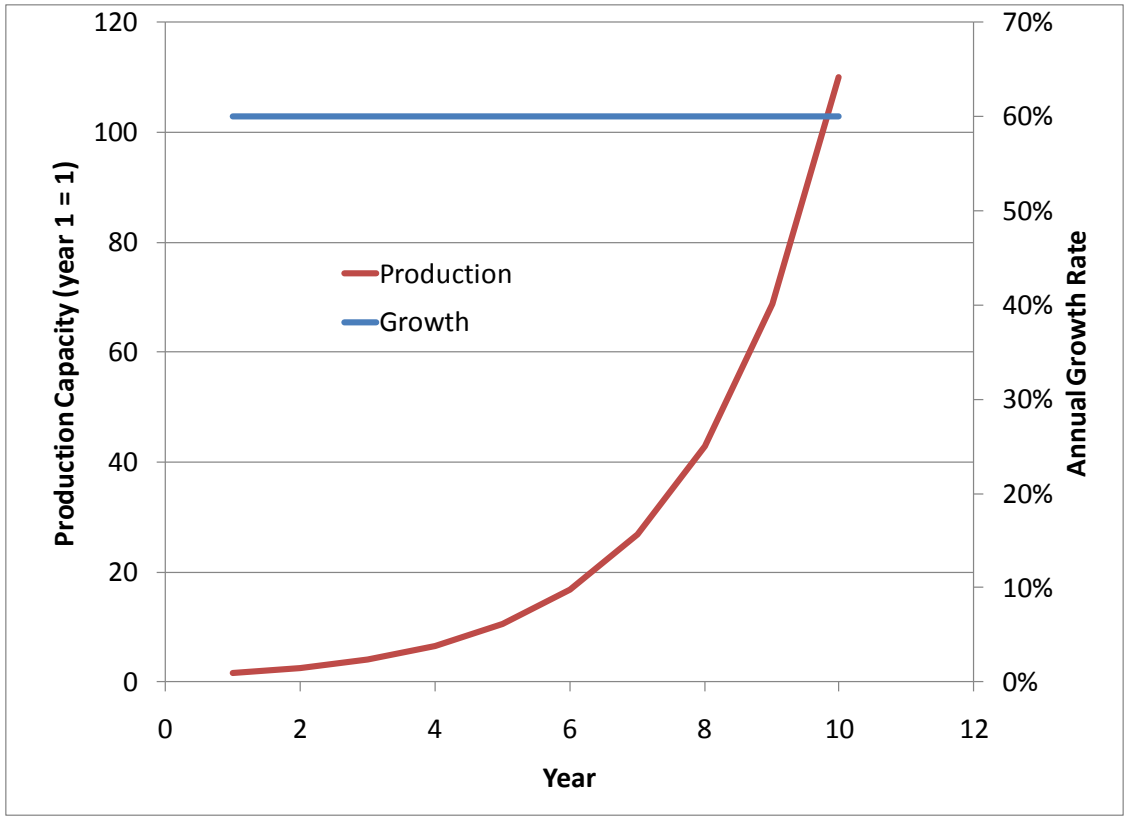
- Order of Magnitude numbers:
- Total pump power 50-200 GW
  - ~ 200 million bars @ 500 W/bar
  - ~ 2 orders of magnitude higher than current supply
- Schedule ~ 8-10 years
  - Subject to congressional funding
- Price target ~ $0.01 / W
  - Includes packaging and lensing
  - ~ 2 orders of magnitude cheaper than today
- ***And this is just for the first plant…***

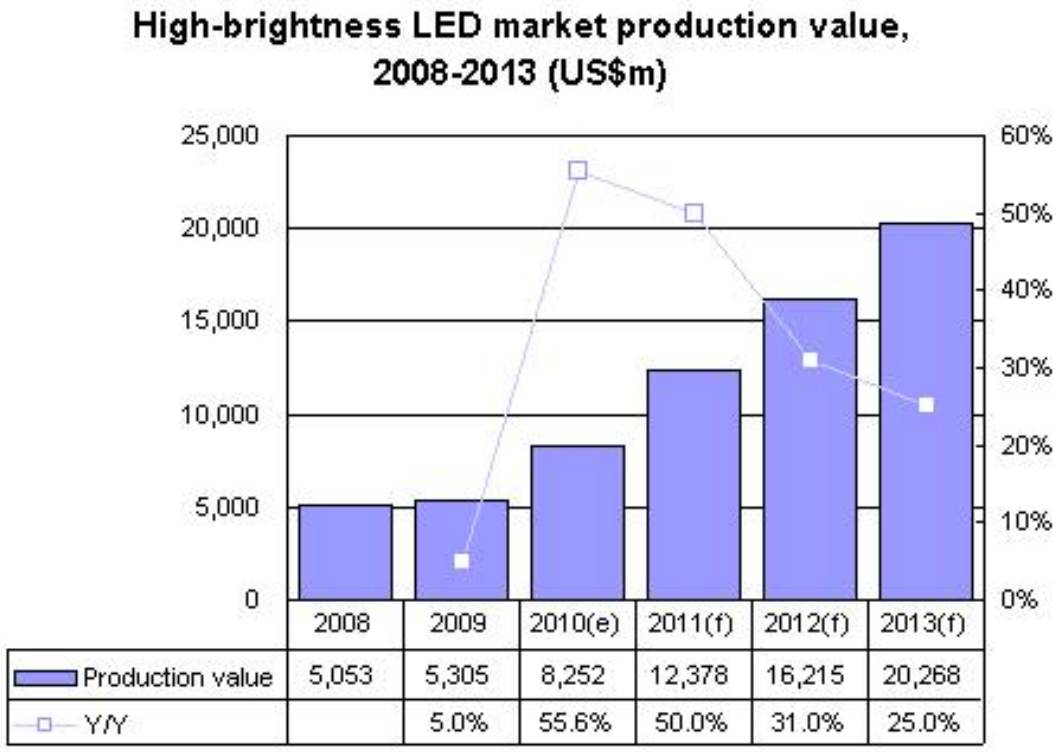
What is required?

- Increasing supply capability by two orders of magnitude requires a ~ 60% AGR for 10 years
- In line with LED ramp-up
  - Much DOE involvement / investment
  - Significant Chinese government investment
- 8-year schedule ➔ 80% AGR
- *If we're going to do this, we need to get started*



LED Examples

- Tremendous increase in LED production
- MOCVD reactor shipments:
  - 2009: ~ 250
  - 2010: ~ 800
  - 2011: ~ 1100
- 50% year-over-year growth in the production value of high-brightness LEDs
- 300-400 reactors/year needed to meet demand
- Chinese subsidies have driven the market
- Lumens/$ is ahead of industry-established roadmap
- Concerns:
  - Oversupply of reactors
  - Undersupply of MOCVD engineers



	2008	2009	2010(e)	2011(f)	2012(f)	2013(f)
Production value	5,053	5,305	8,252	12,378	16,215	20,268
Y/Y		5.0%	55.6%	50.0%	31.0%	25.0%

Sources: DigiTimes
LEDs Magazine
DOE SSL Manufacturing Workshop

Different Thinking

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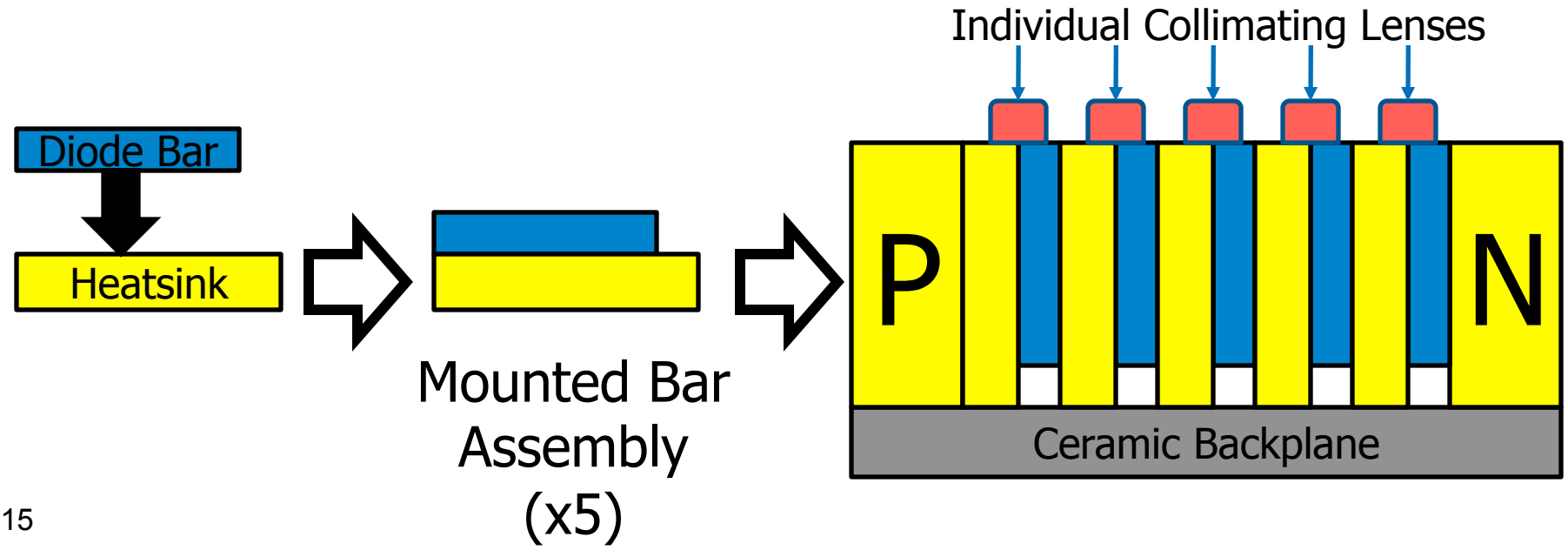
2012	~ 2022
cm edge emitters	• bigger edge emitters • VCSELs / wafer-level processing • not yet invented…
Conventional diode packaging	• High density packaging • Wafer scale
Business driven by science	Business driven by manufacturing
Sequential iterations on existing manufacturing processes	Transition to more LED-like thinking
Current pace of market penetration	Increased market penetration due to lower costs

What would the market look like if diode bars were essentially free?

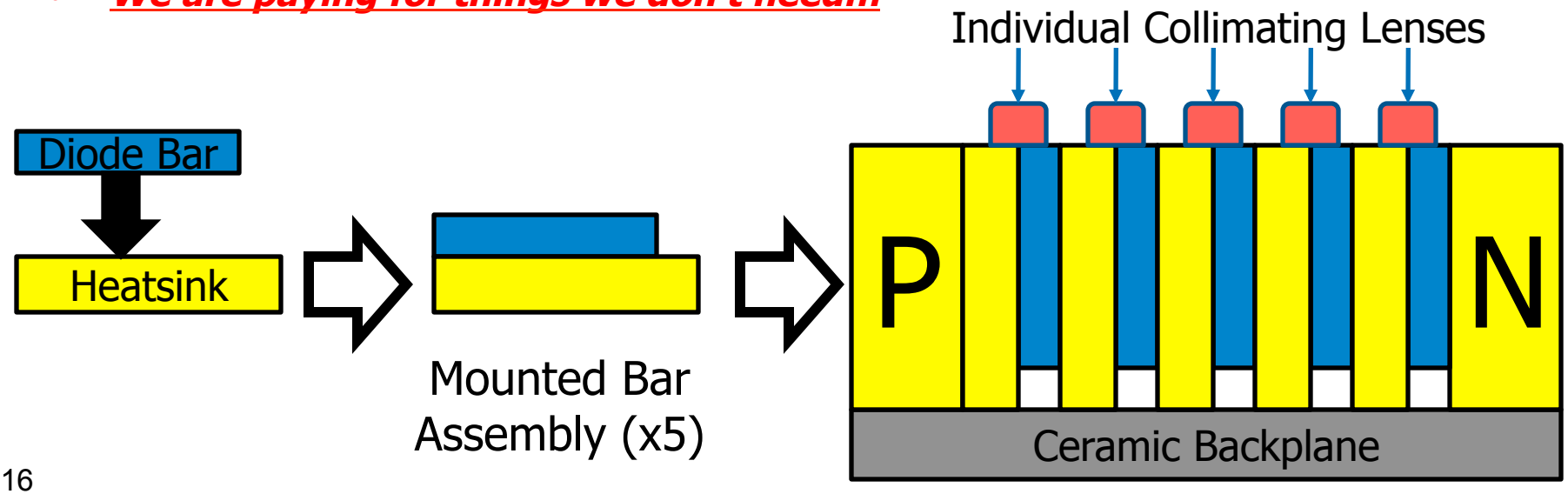
Conventional Diode Packaging

- Power density in a standard array defined by per-bar power and width of heatsink located between bars
- Heatsink cost ~ bar cost
- Lenses individually attached (manually or automatically)
- Even in automated processes, all bars treated as individuals
  - Bar cleaving / singulation
  - Facet coating
  - Packaging



Why do we do this?

- Manufacturing methods developed to meet a wide variety of specifications
- Bars individually mounted to heatsink ➔ Allows for heat dissipation at higher repetition rates (100s-1000s of Hz)
  - Connection to backplane
  - Space between heat sources
- Individual collimating lenses ➔ Facilitates excellent collimation in the fast axis (< 0.15^{o} FWHM)
- Neither of these are required for the current LIFE design, but the costs are still there
- ***We are paying for things we don't need…***



High Density Stack Packaging

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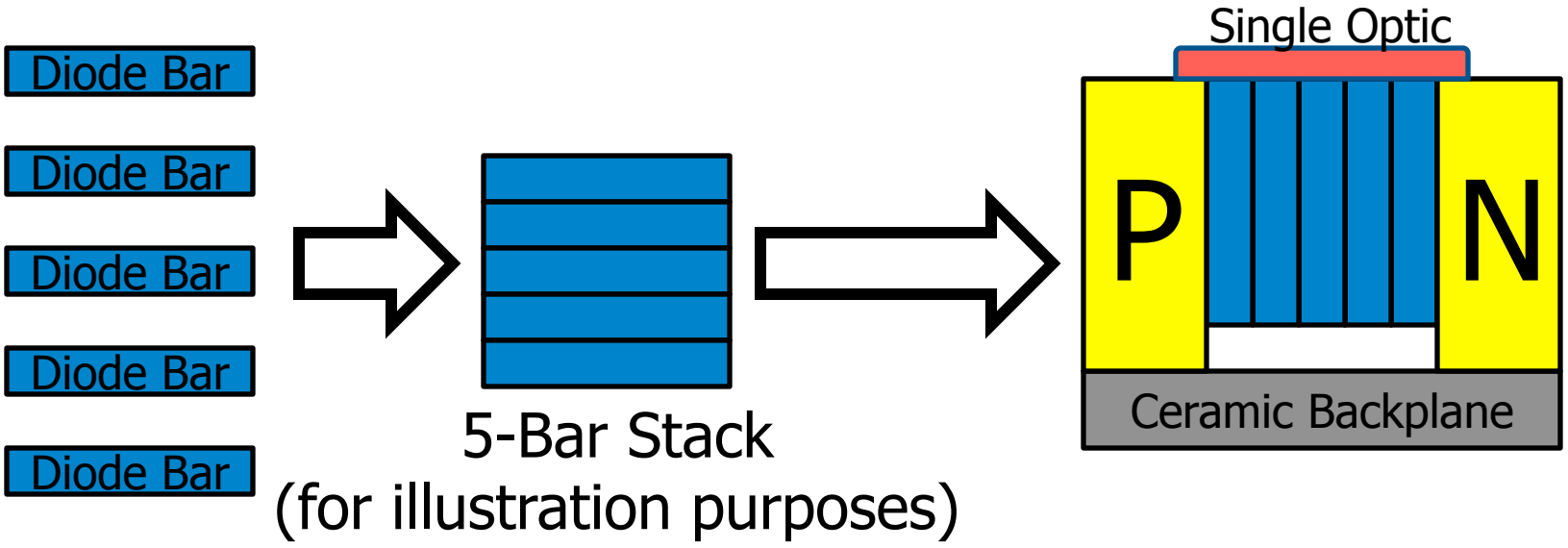
- Low duty cycle of fusion power plants allows for novel packaging
- Elimination of heatsinks reduces cost and increases intensity
- Single optic for stack, engineered to produce required fast-axis divergence
- Arrays can be produced in stack sizes of 20-50 bars
- Drastically increased power density



Array Comparison

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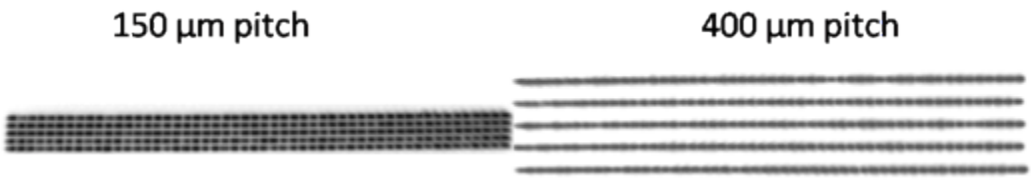
- Difference in packaging & power density clearly seen in photograph and near field image
- NGCEO has been packaging HDS (and variants) for ~ 12 years
- Package is limited only by heatsinking
  - No heat sink between bars
  - ➔ Middle bars run at higher temperatures
  - No effect seen up to ~ 2% duty
- Only possible because of elimination of COD failure mode (elimination of collateral damage)



What does this buy us (cost)?

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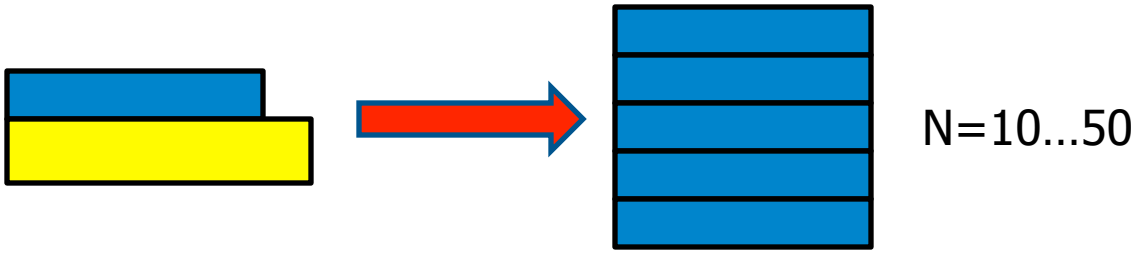
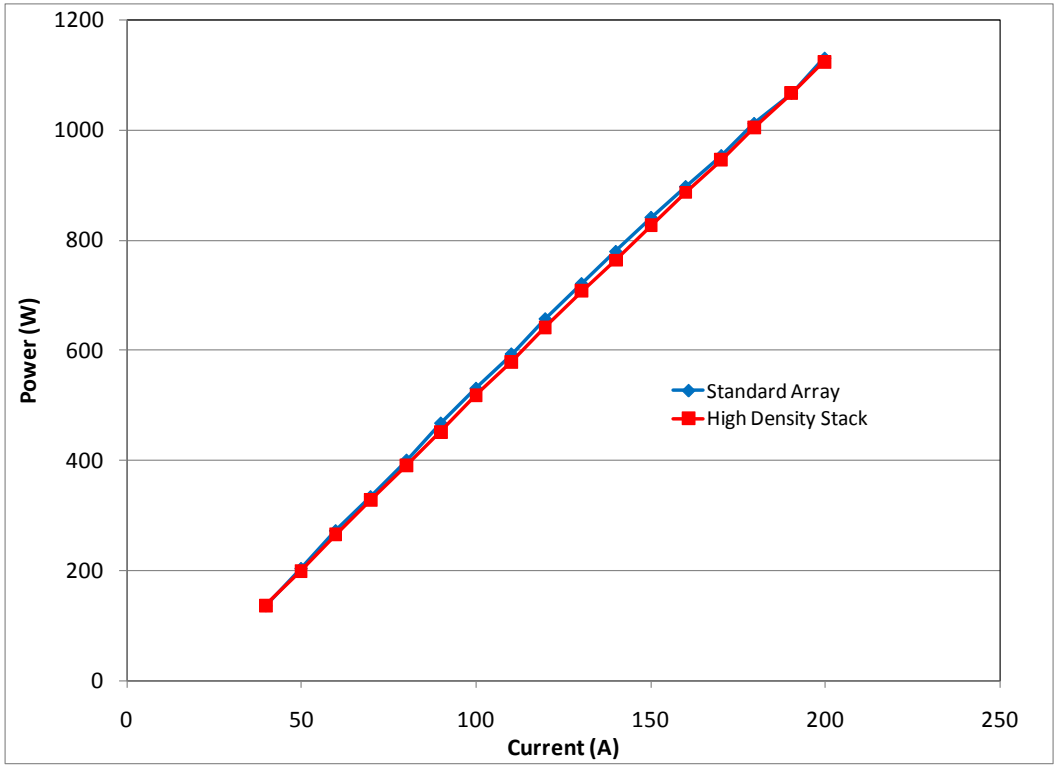
- Elimination of heatsink
  - Reduced material cost
  - Elimination of ~ 50% of solder bonds (alignment, cost)
- Changes the basic building block



  - Changes processing options
  - Build/test/etc. in “blocks” instead of single bars/assemblies

PI Data – High Density Stacks

- PI data for standard and high density stacks shown at right
- 20 Hz, 150 µs
  - Similar duty cycle to typical fusion installations
- No change in slope or threshold observed
- Other test data indicates this is the case up to ~ 2% duty cycle
- Additional optimization will increase operating envelope of this package



Power Density Comparison: High Density Stack vs. Standard Array

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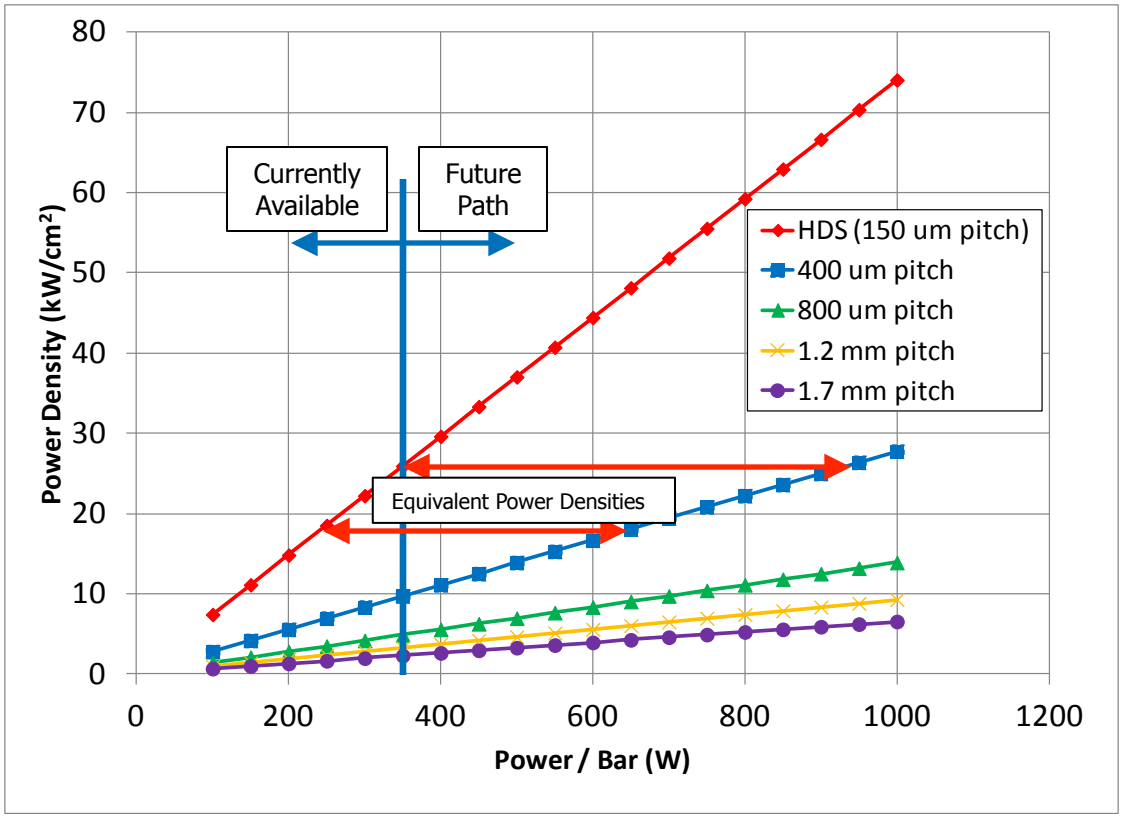
- High Density Stacks offer power densities not available with standard arrays
- HDS @ 150W/bar offers the same power density as 400 µm pitch array @ 400W/bar
- HDS available with same bars as standard arrays
  - Same peak power levels



50-bar HDS @ 500 W/bar

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Specification	Specification	Example Package	Comment
Intensity	25 kW/cm^2	50 kW/cm^2	Higher intensities are available
Efficiency	75%	60+%	Higher efficiency available
Fast-axis divergence	±3 degrees (1/ e^2)	TBD	
MTTF	14 billion shots	>> 14 billion shots	Higher lifetimes are available
Stack Power		25 kW	
# of stacks		400k	
# of bars		200 million	
Total price of diodes		???	

Further Examples

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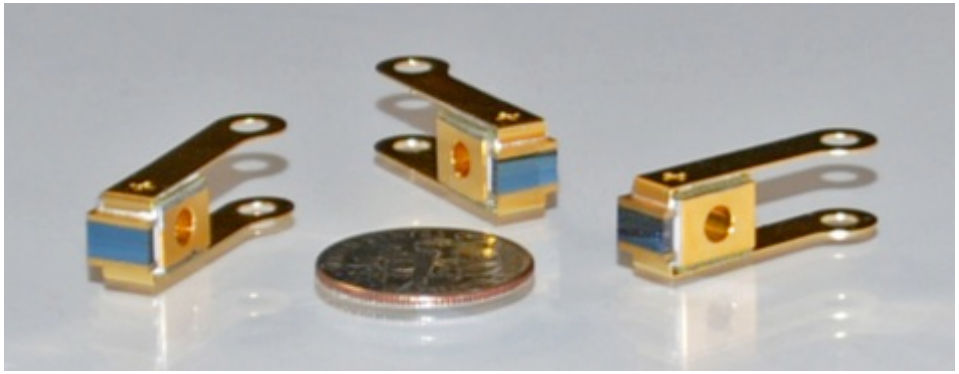
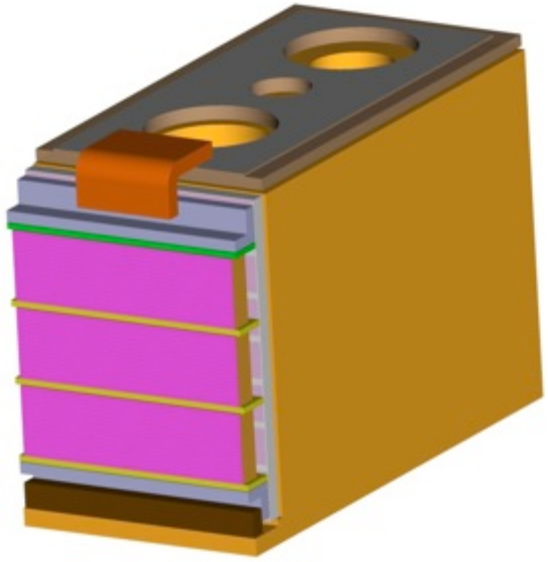
- HDS arrays based on mini-bars
- Segmented HDS arrays
  - 60 bars
  - Design for 15-25 arrays around a thick disk
  - ~ 12kW in 1cm^2





Other Challenges

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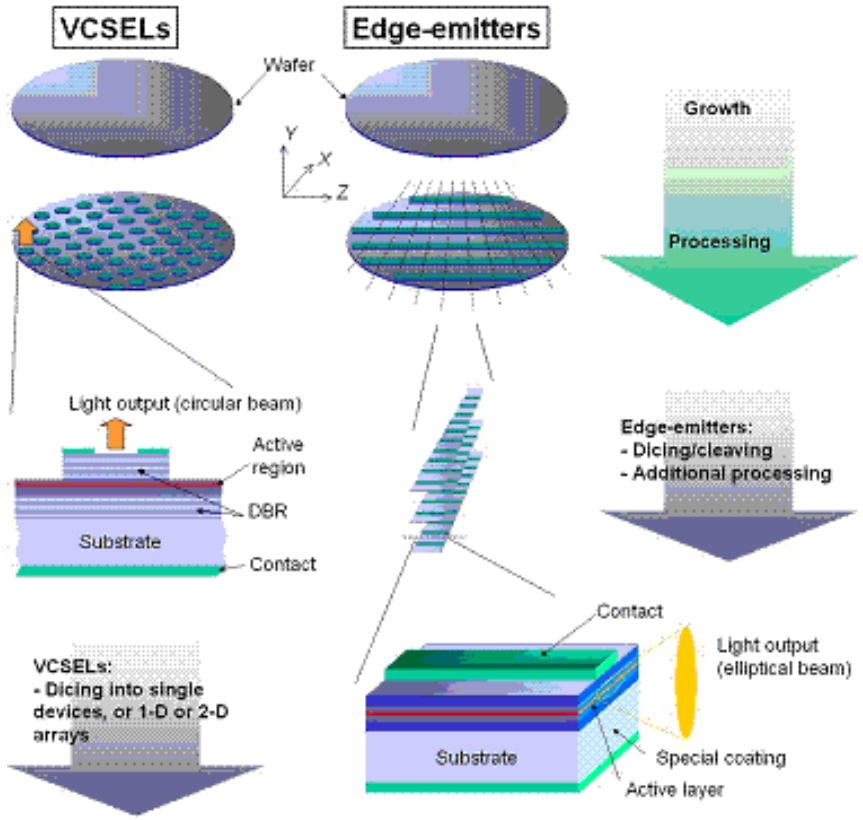
- Every photon requires an electron
  - 500-700W bars ➔ 500-700A drivers
- Diodes packed in close proximity
  - Small drivers located near the array, or
  - A power delivery and inductance nightmare
- Required for production installations
- Required for all diode manufacturers
  - Testing, burn-in, life test, etc.

What about VCSELs?

- Why VCSELs? – Long the "holy grail" of the semiconductor laser field
  - Low-divergence beam
  - Temperature insensitivity (~ 1/5th typical edge emitter)
    - ➔ Simpler cooling requirements
    - ➔ Lower system cost
  - Narrow spectral linewidth
  - Wafer-level processing
    - ➔ Pathway to low device cost



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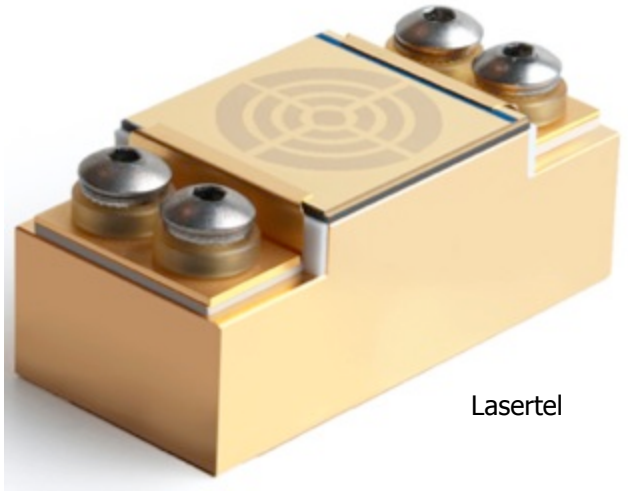
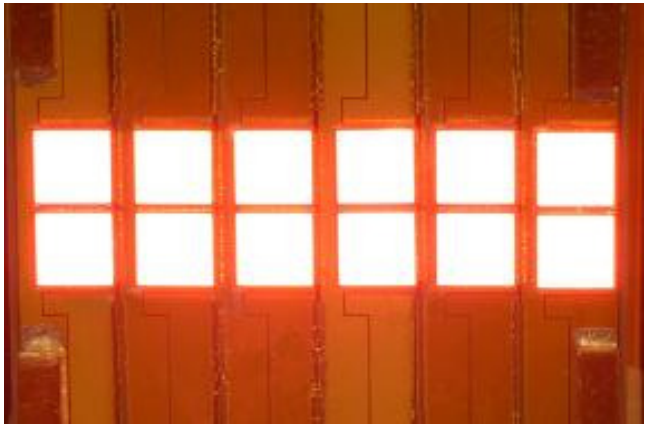
Why not VCSELs?

- Insufficient power density
- Current product offerings:
  - Lasertel: 1kW in 1cm^2 (also 40% PCE)
  - Princeton Optronics: 1.2kW in >1cm^2 (35% PCE)
- Edge-emitters have a big head start:
  - > 1 order of magnitude in power density
  - 1.5-2x in PCE



Lasertel



~ 5.8mm x 20mm
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Conclusions

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- The technical specifications of the LIFE project are directly achievable from today's technology
  - Can be surpassed in many cases
- The technical specs for the arrays may be the easiest part of the whole project, and they're not easy
- Will need LED-like increases in supply chain to make LIFE a reality
- The sooner we start, the sooner we will get there


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